News Release

EDITORIAL/READER CONTACT:
Brian Kiernan, Corporate Communications Manager
Lattice Semiconductor Corporation
503-268-8739 voice
503-268-8193 fax
brian.kiernan@latticesemi.com

LATTICE AND AFFARII DELIVER LOW POWER, LOW COST RRU SOLUTION

HILLSBORO, OR – OCTOBER 26, 2009 – Lattice Semiconductor Corporation (NASDAQ: LSCC) and Affarii Technologies Limited, a solutions provider for networking and telecommunications applications, today announced that they have developed a complete 3G/4G-based Remote Radio Head (RRH) solution for wireless infrastructure customers. This is the first time a full RRH solution has been made available using low power, low cost FPGAs that allows low power RRUs to be deployed without sacrificing flexibility or performance.

Traditionally, near antenna logic for MIMO-based RRH systems has been implemented in high end, premium FPGAs. The high cost and power dissipation of these high end FPGAs has forced vendors to sacrifice design flexibility and attempt expensive ASIC conversions. However, the combination of the industry leading low cost, low power LatticeECP3™ FPGA and Affarii's unique digitalTRX™ technology provides an unprecedented RRH solution that includes Digital Up/Down Converter (DUC/DDC), Crest Factor Reduction (CFR) and Digital Pre-Distortion (DPD) functionality. Additionally, Lattice provides CPRI/OBSAI and Ethernet technology implemented on the ECP3 FPGA's low cost 3G SERDES transceivers.

A Fully Integrated Solution

A fully integrated RRH solution is now available, providing baseband processing for up to two transmit and four receive antennas on a single silicon device, with each antenna supporting four carriers and 20MHz of modulation bandwidth. When used with industry standard Doherty amplifiers, the Digital Predistortion provides up to 30dB of ACLR correction per transmit antenna with PA output efficiencies exceeding 40%. The solution is fully customizable, with end applications including WCDMA, LTE, WiMAX, WiBro, TD-SCDMA and DVB-T/S/H.

The RRH solution is supported by a comprehensive development and test environment that includes GUI-based design simulation, performance analysis and a production test API with design examples. An in-circuit hardware development platform is also being developed.

"The rapid evolution of the wireless infrastructure marketplace means designers must continuously adapt to changing product requirements," said Shane Flint, Managing Director of Affarii Technologies. "Our digitalTRX technology provides DPD and CFR solutions that offer a fast, flexible and cost effective platform for digital transceiver and RRH development. With high ACLR correction and low dynamic power consumption per antenna, designers get both industry leading performance and the flexibility to create the solutions they want."

"Our mid-range LatticeECP3 FPGA family offers our customers an unprecedented combination of low power, high value and the features and performance necessary for sophisticated wireless RRH applications. We are pleased to partner with Affarii to showcase the versatility of the ECP3 FPGA in providing low cost solutions for near antenna logic," said Shakeel Peera, Lattice's Marketing Director for SRAM FPGAs.

About the LatticeECP3 FPGA family

The mid-range LatticeECP3 FPGA family is comprised of five devices that offer standards-compliant multi-protocol 3G SERDES, DDR1/2/3 memory interfaces and high performance, cascadable DSP slices that are ideal for high performance RF, baseband and image signal processing. Toggling at 1Gbps, the LatticeECP3 FPGAs also feature the fastest LVDS I/O available in a mid-range FPGA family, as well as embedded memory of up to 6.8 Mbits.

Logic density varies from 17K LUTs to 149K LUTs with up to 586 user I/O. The LatticeECP3 FPGA family's high performance features include:

• 3.2Gbps SERDES with the ability to mix and match multiple protocols including CPRI, OBSAI, XAUI, Serial RapidIO, PCI Express, 10GbE and SGMII/Gigabit Ethernet on each SERDES quad.

• The SERDES/PCS blocks have been designed specifically to enable the design of the low latency variation CPRI links that are found in wireless basestations with Remote Radio Head connectivity.

• DSP blocks allowing up to 36x36 Multiply and Accumulate functions running at >400MHz. The DSP slices also feature innovative cascadability for implementing wide ALU and adder tree functions without the performance bottlenecks of FPGA logic.

• 1Gbps LVDS I/O, with Input Delay blocks, allows interfacing to high performance ADCs and DACs.

With these features, the LatticeECP3 FPGA solution is ideally suited for deployment in high volume cost- and power-sensitive wireless RRH infrastructure equipment. For more information about this solution, please visit www.latticesemi.com.

Pricing and Availability

The RRH solution is available for demonstration by arrangement with Affarii. Product evaluation kits and development tools will be available in the first quarter of 2010. For more information on pricing and availability please contact sales@affarii.com.

About Affarii Technologies

Affarii is a provider of digital radio and signal processing solutions to the wireless infrastructure and networking marketplace. Affarii's innovative digitalTRX solutions provide a flexible, cost effective and low power solution to digital transceiver development. For more information and product details please visit www.affarii.com

About Lattice Semiconductor

Lattice is the source for innovative FPGA, PLD, programmable Power Management and Clock Management solutions. For more information, visit www.latticesemi.com

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